IN THE CLAIMS:

1. (Original) A method for generating and verifying isolation logic modules in a design of an integrated circuit (IC), the method comprising:

specifying a plurality of voltage constraints defining at least one power domain in the design;

iteratively checking, for each of the power domain, when an isolation logic module isolating the power domain exists in the design;

verifying the correctness of the isolation logic module existing in the design, when the isolation logic module is identified;

generating an isolation logic module for isolating the power domain, when the power domain is not correctly isolated; and

inserting the generated isolation logic in the design.

2. (Original) The method of claim 1, wherein the voltage constraints comprise for each power domain: a corresponding wakeup domain, a wakeup/shutdown signal, and a list of steady state values.

3. (Original) The method of claim 2, wherein each of the steady state values defines a determinable under shutdown conditions.

4. (Original) The method of claim 2, wherein the wakeup/shutdown signal is generated in the wakeup domain.

5. (Original) The method of claim 1, wherein the isolation logic module is in a register transfer level (RTL) description.

6. (Original) The method of claim 1, wherein the design is a RTL description.

7. (Original) The method of claim 1, wherein the voltage constraints are specified by a user by means of a graphical user interface.

8. (Original) The method of claim 1, wherein verifying the correctness of the isolation logic module comprises:

simulating shutdown conditions;

comparing each of the output values of the power domain to a respective steady state value, and generating an error report when the comparison results in an inequality;

determining whether at least one isolation cell in the isolation module is not connected to the wakeup/shutdown signal, and generating the error report when the checking results an affirmative answer; and

in response to detecting the wakeup/shutdown signal being generated in the wakeup domain, generating the error report when the checking results a negative answer; otherwise, generating a success report.

9. (Original) The method of claim 8, wherein the error report comprises at least one of an error type and a cause of the error.

10. (Original) The method of claim 8, wherein the error report and the success report are displayed to the user.

11. (Original) The method of claim 8, wherein the shutdown conditions and the output values of the power domain are highlighted in the design by means of a visualization tool.

12. (Original) The method of claim 8, wherein the isolation cell comprises at least one of an AND gate, an OR gate, and a latch.

13. (Original) The method of claim 1, wherein generating the isolation logic module comprises producing a description language code implementing the isolation logic module.

14. (Original) The method of claim 13, wherein the description language comprises at least one of Verilog, VHDL, and a combination of Verilog and VHDL.

15. (Original) The method of claim 14, wherein the description language code comprises instructions assuring that under shut down conditions each of the output values is equal to a respective steady state value.

16. (Original) The method of claim 13, wherein inserting the isolation logic module comprises:

instantiating the description language code to form an instance of the isolation logic module;

inserting the instance of the isolation logic module in the wakeup domain;

renaming output names of the power domain; and

assigning the original names of output names of the power domain to outputs of the isolation logic module.

17. (Original) The method of claim 16, wherein the insertion of the isolation logic is performed using at least one of back referencing analysis and a synthesized netlist.

18. (Original) The method of claim 17, wherein the synthesized netlist is created using a synthesis tool.

19. (Original) The method of claim 1, wherein inserting the isolation logic module is preceded by verifying the correctness of the isolation logic module placed in the design.

20. (Original) The method of claim 1, wherein at least one of a computer aided design (CAD) system, a CAD program, a netlist voltage domain analysis tool, and a RTL voltage domain analysis tool, is used to implement the method.

21-40. (Canceled).

41. (Original) A method for generating isolation logic modules in a design of an integrated circuit (IC), the method comprising:

specifying a plurality of voltage constraints defining at least one power domain in the design;

iteratively producing, for each of the power domain using the voltage constraints, a description language code implementing the isolation logic module;

instantiating the description language code to form an instance of the isolation logic module;

inserting the instance of the isolation logic module in a wakeup domain;

renaming output names of the power domain; and

assigning the original names of output names of the power domain to outputs of the isolation logic module.

42. (Original) The method of claim 41, wherein the voltage constraints include for each power domain: a corresponding wakeup domain, a wakeup/shutdown signal, and a list of steady state values.

43. (Original) The method of claim 42, wherein the voltage constraints are specified by a user by means of a graphical user interface.

44. (Original) The method of claim 41, wherein the description language comprises at least one of Verilog, VHDL, or combination of Verilog and VHDL.

45. (Original) The method of claim 42, wherein the description language code comprises instructions assuring that under shut down conditions each of the output values is equal to a respective steady state value.

46. (Original) The method of claim 41, wherein the insertion of the isolation logic is performed using at least one of a back referencing analysis and a synthesized netlist.

47. (Original) The method of claim 46, wherein the synthesized netlist is created using a synthesis tool.

48. (Original) The method of claim 41, wherein inserting the isolation logic module is preceded by verifying the correctness of the isolation logic module placed in the design.

49. (Original) The method of claim 41, wherein at least one of a computer aided design (CAD) system, a CAD program, a netlist voltage domain analysis tool, and a RTL voltage domain analysis tool is used to implement the method.

50-58. (Canceled).

59. (Currently Amended) A method for verifying the correctness of isolation logic modules in a design of an integrated circuit (IC), the method comprising:

specifying a plurality of voltage constraints defining at least one power domain in the design;

iteratively simulating shutdown conditions for each ~~of the~~ power domain in the design,

comparing each of the output values of the power domain to a respective steady state value, and generating an error report when the comparison results in an equality;

checking when at least one isolation cell in the isolation module is not connected to a wakeup/shutdown signal, and generating the error report when the checking results in an affirmative answer; and

checking when the wakeup/shutdown signal is generated in a wakeup domain, and generating the error report when the checking results in a negative answer; otherwise, generating a success report.

60. (Original) The method of claim 59, wherein the wakeup domain, the wakeup/shutdown signal, and the steady state values are part of the voltage constraints.

61. (Original) The method of claim 59, wherein the error report comprises at least one of an error type, and a cause of the error.

62. (Original) The method of claim 59, wherein the error report and the success report are displayed to the user.

63. (Original) The method of claim 59, wherein the shutdown conditions and the output values of the power domain are highlighted in the design by means of a visualization tool.

64. (Original) The method of claim 59, wherein the isolation cell comprises at least one of an AND gate, an OR gate, and a latch.

65-75. (Canceled).